REMARKS

The application has been reviewed in light of the Office Action dated January 12, 2007. Claims 1-58 are pending in this application, with claims 1, 12, 18, 24, 28, 39, 50, and 51 being in independent form. By the present Amendment, claims 1 and 50 have been amended. It is submitted that no new matter has been added and no new issues have been raised by the present Amendment.

Applicants acknowledge the Examiner's determination that claims 31, 33-36, 42, 44-47, 54, 55, 56, and 58 represent allowable subject matter and would be allowable if rewritten in independent form.

Claims 1-11 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,987,632 (Irrinki). Claims 12-15, 18-21, 28, 32, 39, 43, 50, 51, and 57 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Irrinki in view of U.S. Patent No. 5,710,550 (Hseih). Claims 16, 17, 22, 23, 37, 38, 48, and 49 were rejected under 35 U.S.C. § 102(a) as allegedly obvious over Irrinki in view of Hseih and U.S. Patent No. 5,361,232 (Petschauer). Claims 24-27, 29, 40, and 52 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Irrinki in view of Hseih and U.S. Patent No. 3,409,828 (Kelsey). Kelsey is not of-record in this case and the Applicants assume that the Office Action indented to cite U.S. Patent No. 4,173,029 (Rabindran). Claims 30, 41, and 53 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Irrinki in view of Hseih, Rabindran and Microsoft Computer Dictionary, fifth edition (Dictionary).

Independent claim 1, as amended, relates to a semiconductor memory device including an array of memory cells arranged in rows and columns. The device also includes means for

selecting the memory cells of the array in a repair unit in a test operation mode. The device includes means for supplying a power voltage to the selected memory cells in the test operation mode and cutting off power to remaining memory cells in the test operation mode.

This claim has been amended hereby to emphasize that during the test operation mode, power is supplied to the selected memory cells and power is cut off to the remaining memory cells.

The Examiner contends that Irrinki teaches cutting off power to the remaining memory cells because Irrinki, at column 9, lines 26-61, relates to blowing fuses to individual rows and columns. However, the cited portions of Irrinki, best illustrated at Step 550, Figure 5, relates to blowing fuses to individual rows and columns for those memory cells that have already been tested and have been determined to be failing cells. By blowing the fuses to the failing cells, the "failures that may only exist under a particular set of operating conditions" are converted to "functional failures." In a sense, Irrinki performs a stress test on the cells and those cells that fail the stress test are cut off by blowing the respective fuses so that weak cells do not fail later on. It is inherent in this concept, and is clearly shown by Figure 5, that the fuses are blown ***after*** the test has been completed. While in independent claim 1, power is cut off to the remaining memory cells ***during the test operation mode***. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 1, as amended, is patentably distinct from the cited art. Similarly, dependent claims 2-11 are patentably distinct from the cited art at least owing to their dependency upon independent claim 1.

Similarly, in independent claim 12, the remaining second power lines are disconnected from the first power line, ***in the test operation mode***. In holding that Irrinki teaches this claim

element, the same rational is put forth, namely, that blowing fuses to individual rows and columns is analogous to disconnecting the remaining second power lines from the first power line, in the test operation mode. As shown above, in Irrinki, the fuses are blown ***after*** the test has been completed. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 12 is patentably distinct from the cited art. Similarly, dependent claims 13-17 are patentably distinct from the cited art at least owing to their dependency upon independent claim 12.

Similarly, in independent claim 18, the remaining second power lines are disconnected from the first power line, ***in the test operation mode***. Accordingly, independent claim 18 is patentably distinct from the cited art for at least similar reasons to those discussed above. Dependent claims 19-23 are patentably distinct from the cited art at least owing to their dependency upon independent claim 18.

Similarly, in independent claim 24, the remaining third power lines are disconnected from the second power line, ***in the test operation mode***. Accordingly, independent claim 24 is patentably distinct from the cited art for at least similar reasons to those discussed above. Dependent claims 25-27 are patentably distinct from the cited art at least owing to their dependency upon independent claim 24.

In independent claim 28, a switch circuit connects a second power line to a first power line in response to the selection signals, in a test operation mode. The Office Action suggests that this feature is taught by Irrinki at col. 9, lines 51-62. The Office Action further suggests that the cited portion of Irrinki teaches this feature by holding that "voltage tests may be performed on each row and column individually." While the cited portion of Irrinki relates to the performance

of multiple stress tests upon the memory storage device to detect failing rows and columns, the cited portion of Irrinki fails to indicate that each row and column are checked individually. Instead, the cited portion of Irrinki holds that the memory storage device is tested with "various read and write patterns" implying that multiple rows and columns of memory are simultaneously tested using the read and write patterns. While such testing may be able to indicate which rows and columns are failing, this is not equivalent to testing "each row and column individually" as the former does not require electrical isolation.

Moreover, assuming arguendo that Irrinki did teach "voltage tests may be performed on each row and column individually" this does not amount to a teaching or suggestion that a switch circuit connects a second power line to a first power line in response to the selection signals, in a test operation mode. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 28 is patentable distinct from the cited art. Similarly, dependent claims 29-38 are patentably distinct from the cited art at least owing to their dependency upon independent claim 28.

In independent claim 39, a switch circuit connects a second power line to a first power line in response to selection signals and disconnects the remaining second power lines from the first power line, in a test operation mode. The Office Action suggests that this feature is taught by Irrinki at col. 9, lines 51-62. The Office Action further suggests that the cited portion of Irrinki teaches this feature by holding that "voltage tests may be performed on each row and column individually." While the cited portion of Irrinki relates to the performance of multiple stress tests upon the memory storage device to detect failing rows and columns, the cited portion of Irrinki fails to indicate that each row and column are checked individually. Instead, the cited portion of

Irrinki holds that the memory storage device is tested with "various read and write patterns" implying that multiple rows and columns of memory are simultaneously tested using the read and write patterns. While such testing may be able to indicate which rows and columns are failing, this is not equivalent to testing "each row and column individually" as the former does not require electrical isolation.

Moreover, assuming arguendo that Irrinki did teach "voltage tests may be performed on each row and column individually" this does not amount to a teaching or suggestion that a switch circuit connects a second power line to a first power line in response to selection signals and disconnects the remaining second power lines from the first power line, in a test operation mode. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 39 is patentably distinct from the cited art. Similarly, dependent claims 40-49 are patentably distinct from the cited art at least owing to their dependency upon independent claim 39.

In independent claim 50, as amended, a power voltage is supplied to the selected memory cells in the test operation mode in response to the selection signals and power-supply to the remaining memory cells is cut off ***in the test operation mode***. As described above, with respect to claim 1, in Irrinki, the fuses are blown ***after*** the test has been completed. While in independent claim 50, power-supply to the remaining memory cells is cut off ***in the test operation mode***. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 50 is patentably distinct from the cited art.

In independent claim 51, a switch circuit connects a second power line to a first power line in response to selection signals, in a test operation mode. The Office Action suggests that

this feature is taught by Irrinki at col. 9, lines 51-62. The Office Action further suggests that the cited portion of Irrinki teaches this feature by holding that "voltage tests may be performed on each row and column individually." While the cited portion of Irrinki relates to the performance of multiple stress tests upon the memory storage device to detect failing rows and columns, the cited portion of Irrinki fails to indicate that each row and column are checked individually. Instead, the cited portion of Irrinki holds that the memory storage device is tested with "various read and write patterns" implying that multiple rows and columns of memory are simultaneously tested using the read and write patterns. While such testing may be able to indicate which rows and columns are failing, this is not equivalent to testing "each row and column individually" as the former does not require electrical isolation.

Moreover, assuming arguendo that Irrinki did teach "voltage tests may be performed on each row and column individually" this does not amount to a teaching or suggestion that a switch circuit connects a second power line to a first power line in response to a selection signals, in a test operation mode. Moreover, the remainder of the cited art fails to teach or suggest this claim feature. Accordingly, independent claim 51 is patentable distinct from the cited art. Similarly, dependent claims 52-58 are patentably distinct from the cited art at least owing to their dependency upon independent claim 51.

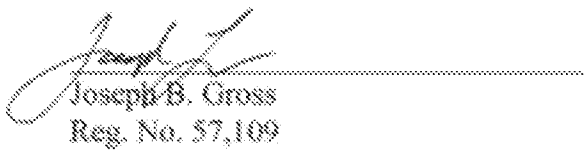
The Office is hereby authorized to charge any additional fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,



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